REMARKS

Claims 38, 45-51, and 62 are pending in the present application. In the Office Action dated November 28, 2005, claims 38, 45, 46, 49, 52-54, 57, 62 and 63 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,204,137 to Teo et al. ("Teo"). Claims 47, 48, 50, 51, 55, 56, 58 and 59 were rejected under 35 U.S.C. 103(a) as being unpatentable over Teo in view of U.S. Patent No. 6, 130,102 to White, Jr. ("White").

In Figures 9 and 10, Teo discloses a semiconductor structure including a substrate 70 having spaced apart STI regions 86 distributed over the substrate 70 with source and drain junctions 110 formed in the substrate 70 between adjacent STI regions 86. The flanks of each of the STI regions 86 have sidewall spacers 110. As best shown in Figure 10, an epitaxial silicon layer 111 is selectively grown over the source and drain junctions 110. Each sidewall of the epitaxial silicon layers 111 abut an opposing surface of an adjacent sidewall spacer 110. Thus, the sidewall spacers 110 appear to provide an important function of at least partially defining the ultimate geometry of the epitaxial silicon layer 111.

In contrast, the embodiment of an in-process substrate shown in Figure 2 of the present application has epitaxial grown contacts 200, 202, and 204 that are free standing and the sidewall surfaces thereof do not abut another surface.

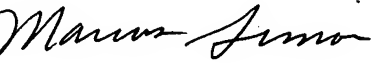
Turning now to the claims, the patentably distinct differences between the cited references and the claim language will be specifically pointed out. Claim 38 recites "[a]n in-process substrate structure including a plurality of contact regions and a plurality of non-contact regions adjacent the contact regions on a surface of the substrate, the in-process substrate structure comprising: a selectively formed single crystal contact on each single crystal contact region, each single crystal contact being isolated from single crystal contacts on adjacent contact regions, each single crystal contact having an arcuate, convex upper surface intersected by two sidewall surfaces, the two sidewall surfaces being substantially perpendicular to the surface of the substrate, *each of the two sidewall surfaces do not abut another surface.*" (Emphasis Added). As discussed in more detail above, Teo fails to disclose or fairly suggests at least one single crystal contact having the recited structure in which the sidewall surfaces thereof do not abut another surface as required by claim 38. In contrast, the sidewall surfaces of the single crystal contact disclosed in Teo (epitaxial silicon layer 111) clearly abuts another surface,

namely, the surface of the sidewall spacers 102. Therefore, claim 38 is not anticipated by Teo. Claims depending from claim 38 are also allowable due to depending from an allowable base claim and further in view of the additional limitations recited in the dependent claims.

All of the claims remaining in the application (i.e., claims 38, 45-51, and 62) are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



Marcus Simon
Registration No. 50,258
Telephone No. (206) 903-8787

MS:clr

Enclosures:
Postcard
Fee Transmittal Sheet (+ copy)

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)

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